# P2C 2014



# On how to efficiently exploit reconfiguration aspects from your design The FASTER tool chain

Parallel and Pervasive Computing Week 2014

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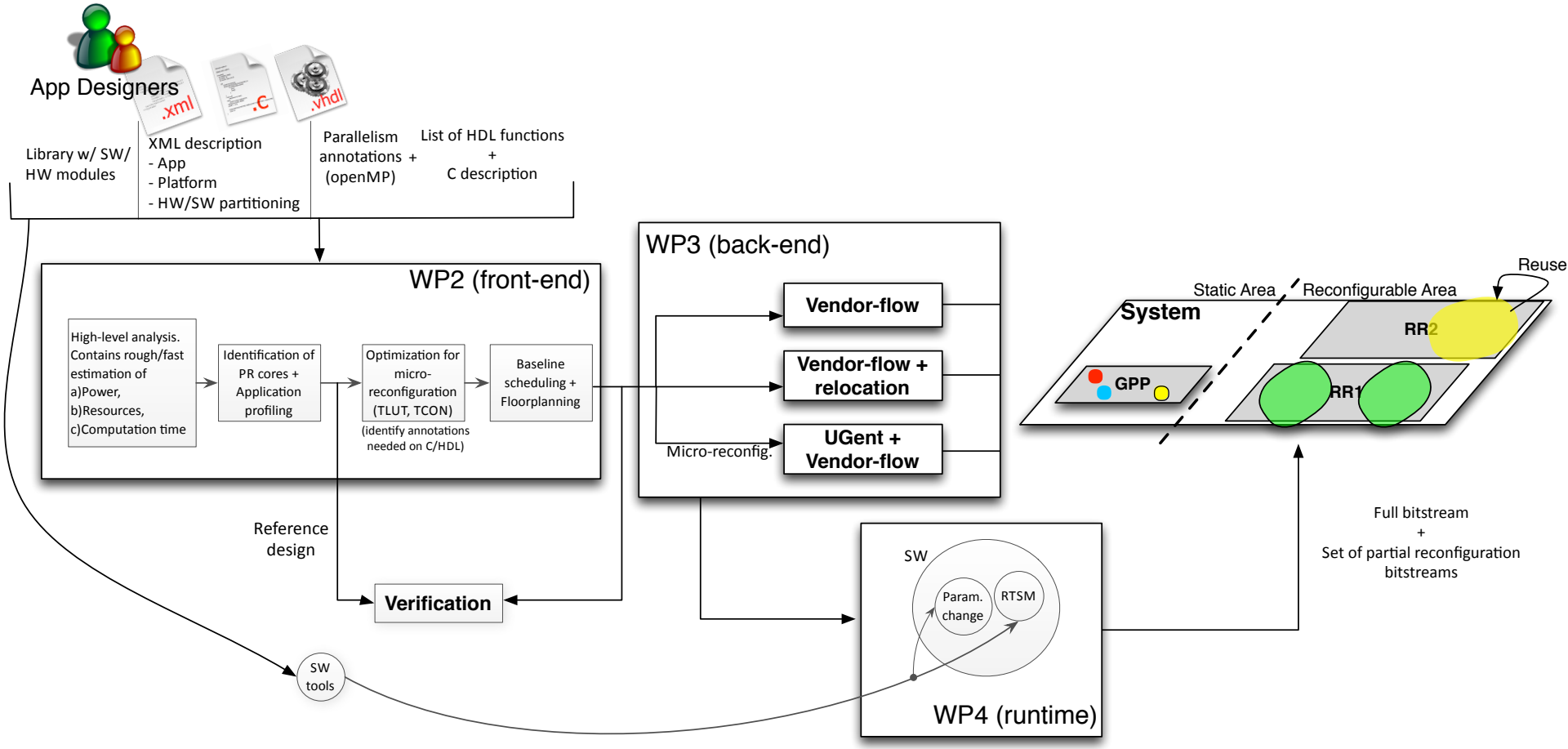
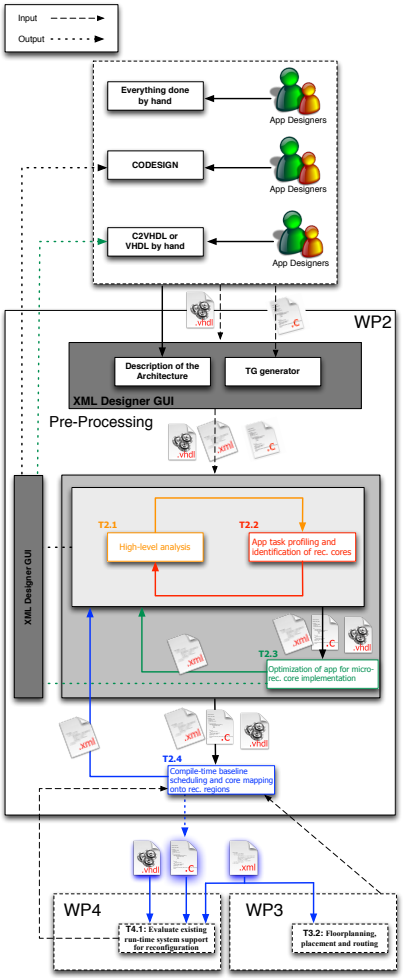
# The FASTER Project

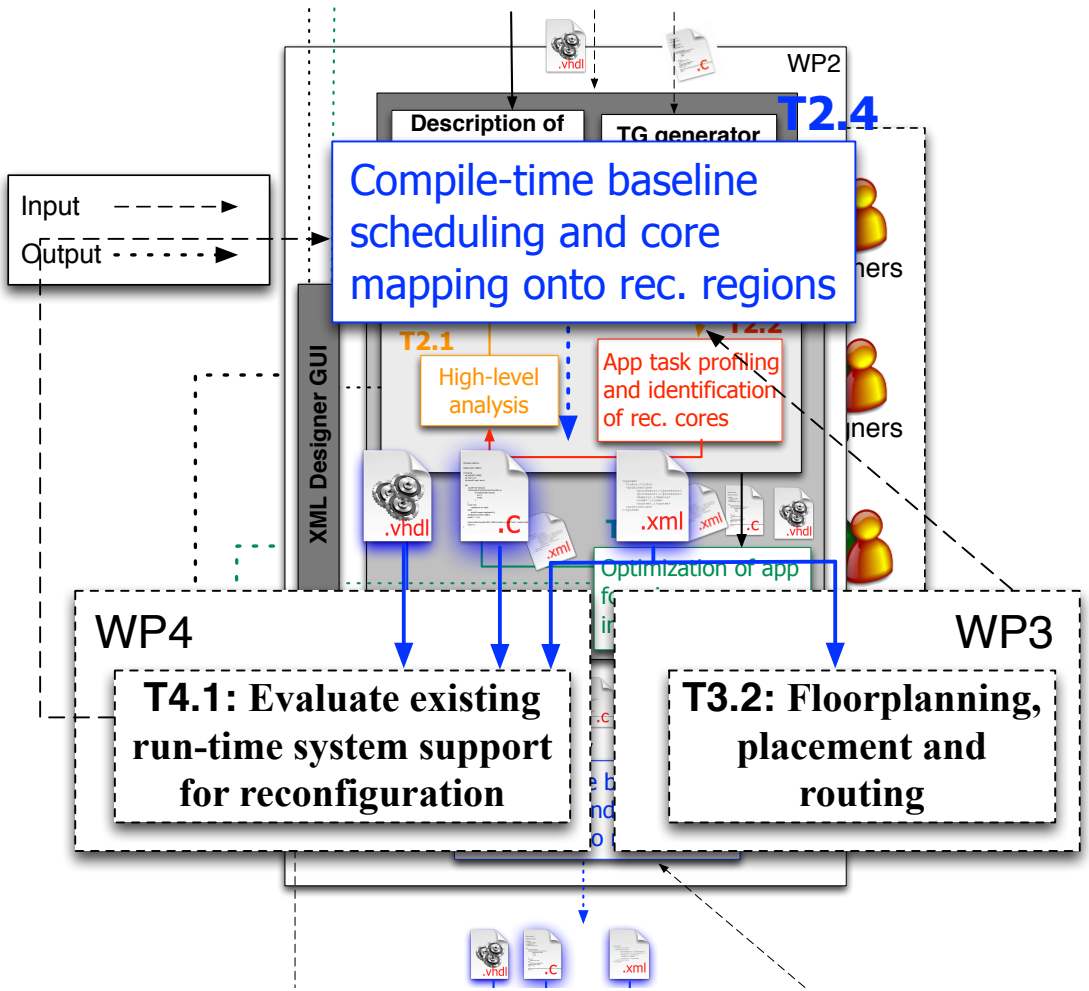


# FASTER front-end: goals

- Analyze each application and:
  - Define its components
    - HW/SW, reconfigurable HW modules, …
  - Estimate, identify, and optimize its performance and constraints on the target reconfigurable computing system
    - Execution time, floorplanning and placement, HW/SW execution, …
- How to do it? Identifying:
  - The partitioning of the input specification in HW/SW components
  - The implementation(s) of the modules to be realized as HW accelerators
  - The corresponding *level* of reconfigurability for HW components
    - none, micro, region based
  - The power constraints
  - The floorplanning constraints
    - size and shape
  - The placement requirements
  - The baseline schedule for application's execution

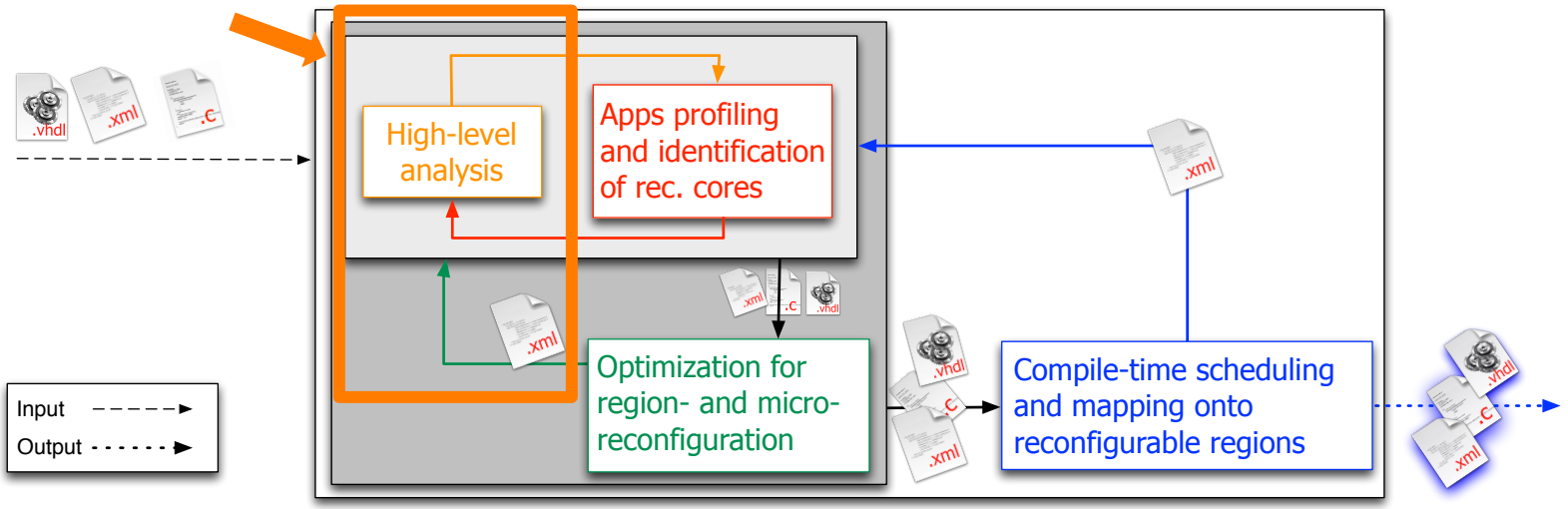
# FASTER front-end: proposed flow



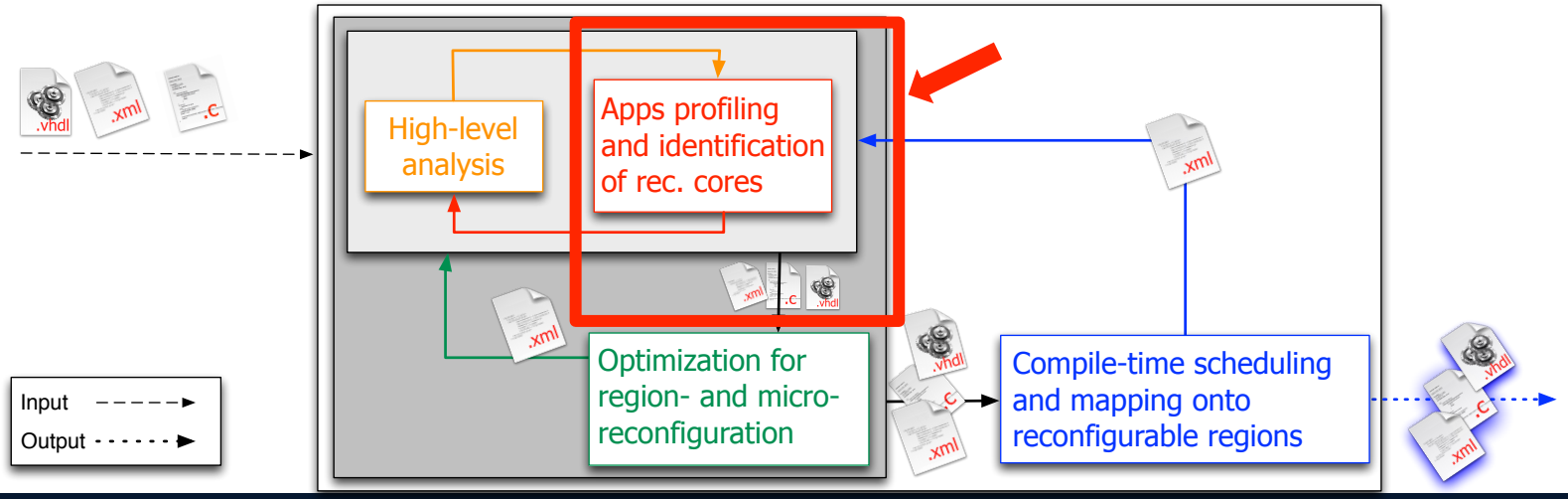
# High-level analysis

- Identify reconfiguration opportunities
- Analyze run-time benefits for stencil computation
- Evaluate run-time solutions



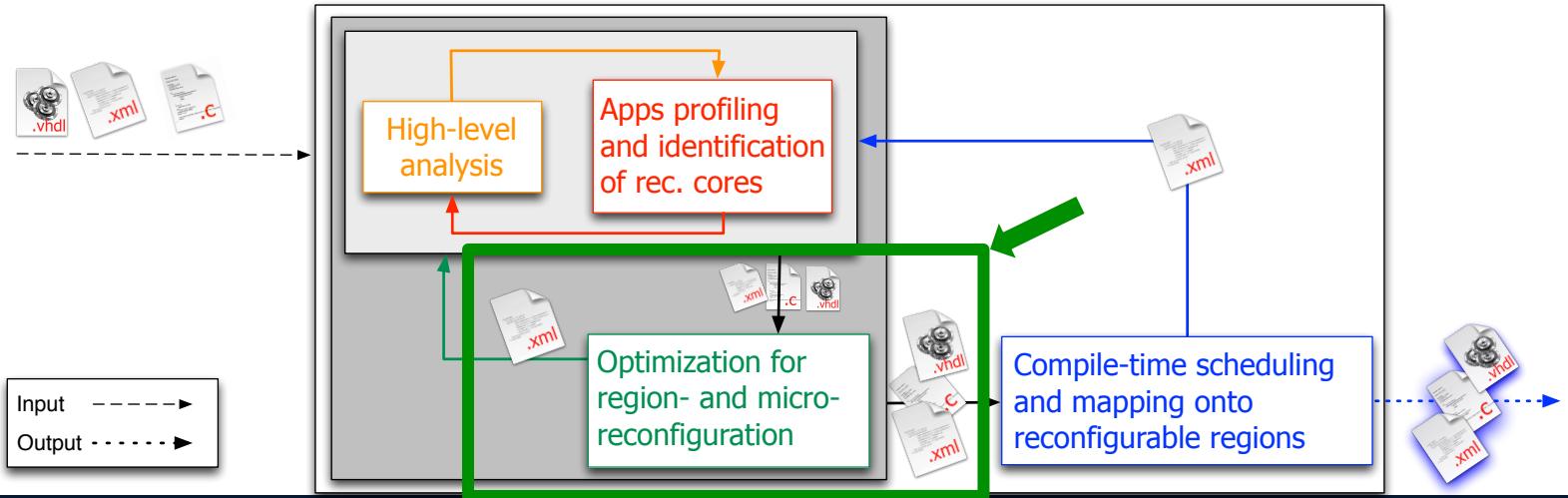
# Application task profiling and identification of reconfigurable cores

- Analysis of the application to improve the performance by exploiting the cores and the reconfiguration capabilities of the architecture
  - Task graph restructuring to improve the performance
  - Generation of the necessary data for the target specifications
  - Management of multiple implementation per tasks
  - HW/SW mapping of the resulting tasks on the different components and reconfigurable areas



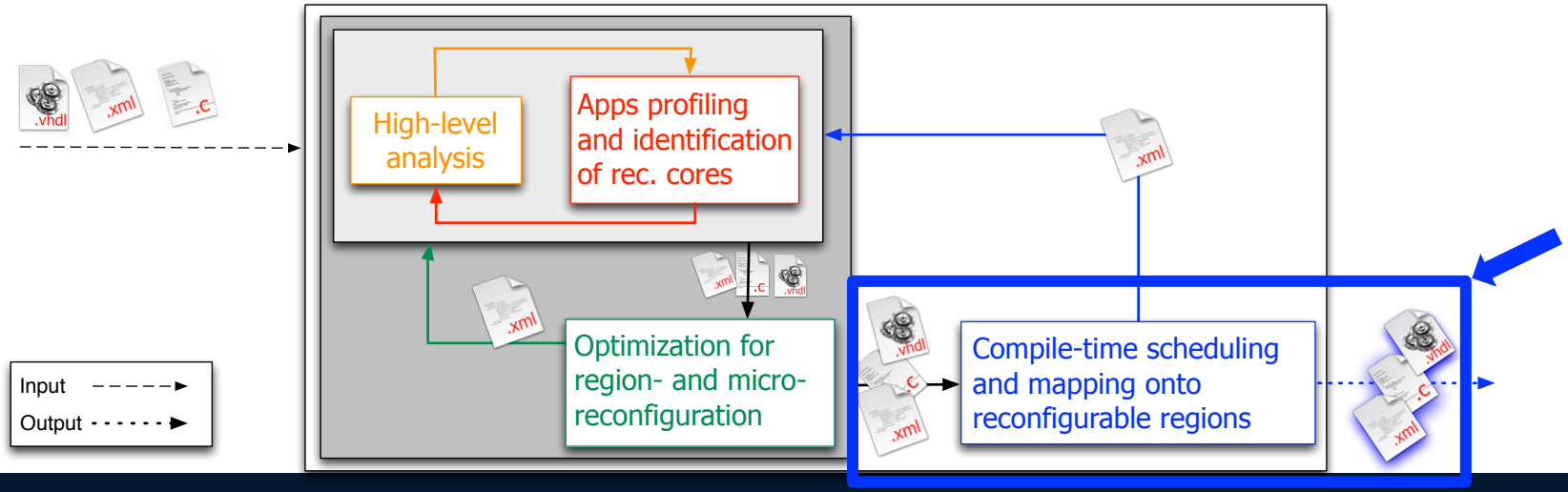
# Optimization of applications for micro-reconfigurable core implementation

- Optimize the applications for micro-reconfiguration implementation
  - Study and increase the parameter value 'locality' in time
  - Research how current applications can be altered to benefit more from micro-reconfiguration
  - Investigate multi-mode applications



# Compile-time baseline scheduling and core mapping onto reconfigurable regions

- Identify the floorplanning constraints (e.g., size and shape) and the corresponding placement requirements
- Implement a heuristic reconfiguration-aware scheduler, used as a baseline schedule for application's execution



# Tutorial agenda

- Optimization of applications for micro-reconfigurable core implementation
  - Dirk Stroobandt, Univeristy of Ghent [2pm – 3pm]
- Application task profiling and identification of reconfigurable cores
  - Riccardo Cattaneo, Politecnico di Milano [3pm – 3.30pm]

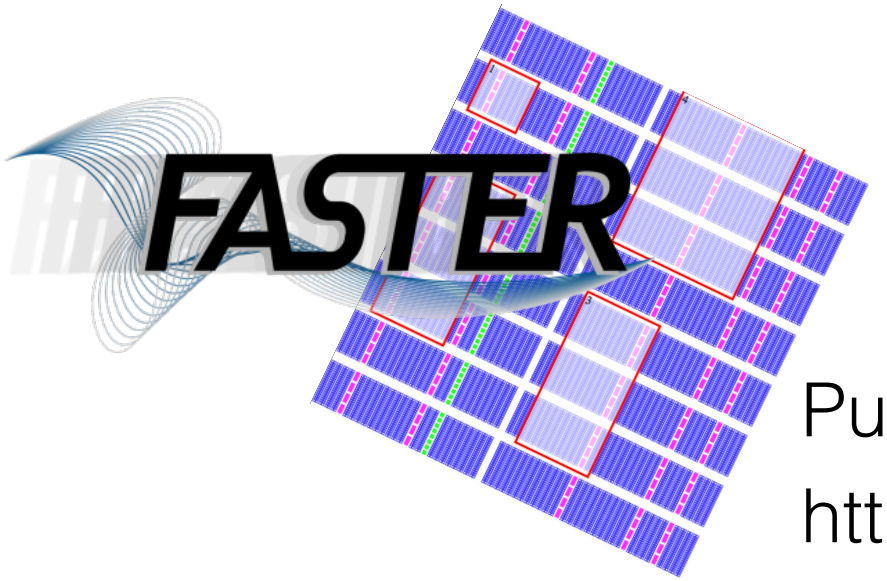
- Coffee Break 3.30pm – 4.00pm

- Application task profiling and identification of reconfigurable cores
  - hands-on experience on theprivate  FASTER VM
  - Riccardo Cattaneo, Politecnico di Milano [4pm – 5pm]
- Compile-time baseline scheduling and core mapping onto reconfigurable regions
  - hands-on experience on the online public available FASTER VM
  - Marco Rabozzi, Politecnico di Milano [4pm - 5pm]

# Questions


EU Project

http://www.fp7-faster.eu/




Public available tool

http://floorplacer.necst.it/